USN | | | | | | | | | | |

06CS32

Third Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Sketch and explain the circuits of a combination clipper which limit the output between ± 10 V. Assume the diode voltage is 0.7 V. **(08 Marks)**

b. With neat diagram and waveforms explain the working of a negative clamper and also write the condition for stiff clamper. **(08 Marks)**

c. Explain how charge storage is overcome in Schottky diodes. **(04 Marks)**

2 a. Explain small signal operation of amplifiers **(06 Marks)**

b. What is the significance of ac emitter resistance in common emitter amplifier? **(04 Marks)**

c. Calculate the input impedance of the base in Fig. Q 2(c) with β = 150 also draw the ac equivalent circuit using π model. **(10 Marks)**

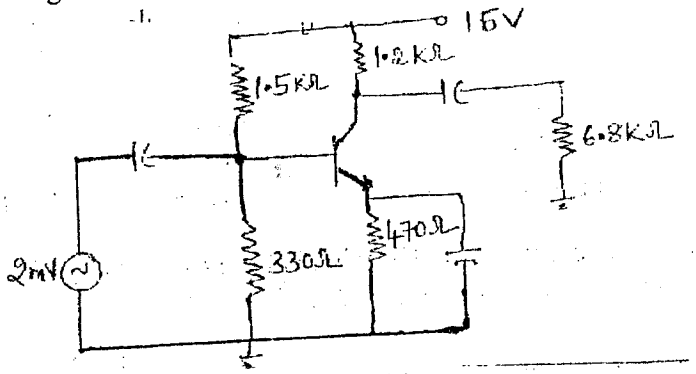


Fig. Q 2(c)

3 a. With a neat sketch explain the working of a swamped amplifier and derive the expressions for voltage gain and input impedance of the base. **(10 Marks)**

b. Calculate the output impedance of the amplifier in Fig. Q 3(b). **(06 Marks)**

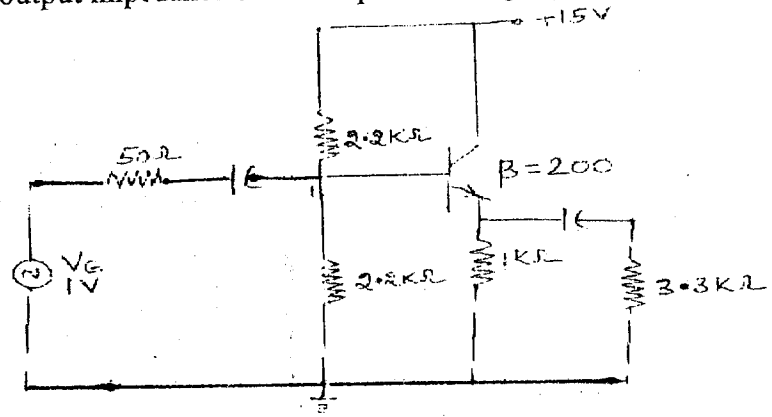


Fig. Q 3(b)

c. Write a note on complementary Darlington pair. **(04 Marks)**

4 a. Explain the working of class B push pull emitter follower, [illegible] AC load lines. (10 Marks)

b. Calculate the efficiency and [illegible] for power dissipation [illegible] amplifier shown in Fig. Q 4(b) if the peak to peak output voltage [illegible] the base is 100Ω.

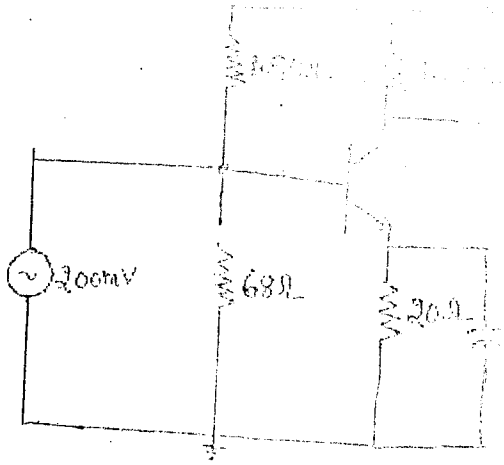


Fig. Q4(b)

(10 Marks)

5 a. Describe the drain curves and Transconductance curve of enhancement mode MOSFET. (08 Marks)

b. Explain active load switching. How it advantages over passive load switching? (06 Marks)

c. With a neat circuit diagram explain CMOS inverter. (06 Marks)

6 a. Draw the frequency response of an AC amplifier. Define the terms cut off frequency, mid band gain. Derive the expression for gain in terms of mid band gain and cut off frequencies. (06 Marks)

b. OP Amp 74 IC has a mid band gain of 100,000, lower cut off frequency of 10 Hz and roll of rate 20 dB per decade. What is the voltage gain at 10 kHz? (06 Marks)

c. Explain ICVS amplifier. (08 Marks)

7 a. Design an OP Amp relaxation oscillator for a frequency of 1 kHz. Also draw the output waveform and waveform across the capacitor. (10 Marks)

b. Write the functional block diagram of IC 555 timer. Explain astable operation with the circuit diagram. Also draw the output waveform and waveform across the capacitor. (10 Marks)

8 a. Define load regulation, line regulation and output resistance for a voltage regulator. For a regulator the measured values are V_{NL} = 9.91 V, V_{HL} = 9.81 V, V_{HL} = 9.94 V and V_{LL} = 9.79 V. Calculate the load regulation and line regulation. (10 Marks)

b. What are switching regulators? Explain buck regulator. (10 Marks)

*****

USN | | | | | | | | | | |

06CS32

Third Semester B.E. Degree Examination, June / July 08
Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions, choosing atleast two questions from each part.***

PART - A

1 a. Explain the working of a negative clipper with its ct diagram. **(05 Marks)**

b. Sketch the wave form output V_{out} in the following circuit, indicating the values of maximum positive and negative output voltages.

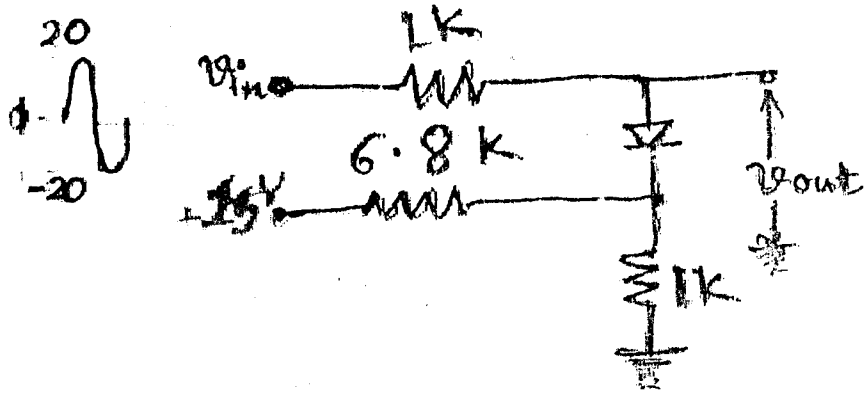


Fig. Q 1(b) **(05 Marks)**

c. Explain the working of a positive clamper with suitable diagrams. **(05 Marks)**

d. Explain the working of Schottkey diode. **(05 Marks)**

2 a. What is the ac collector voltage in the first stage of the amplifier circuit shown in Fig. Q 2(a)? Calculate the output voltage V_{out} across the load resistor.

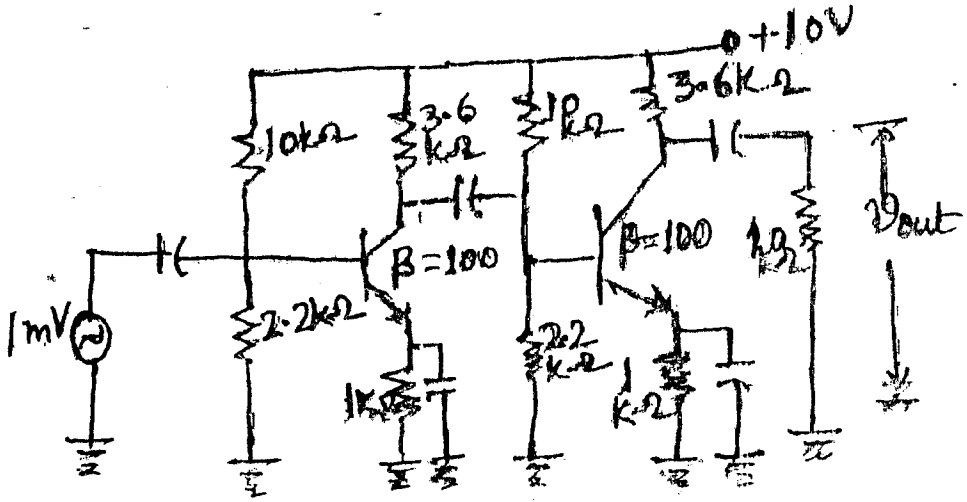


Fig. Q 2(a) **(10 Marks)**

b. Draw the circuit diagram of a swamped amplifier. Write down its ac equivalent circuit and derive expressions for Zin (base) and voltage gain A_v. **(10 Marks)**

3 a. With the help of a circuit diagram, explain the working of a voltage divider biased (VDB) amplifier, highlighting on bias stabilization. (08 Marks)

b. In the following circuit, what is the value of capacitor 'C' needed to efficiently short the point E to ground, if the input frequency is 1 kHz?

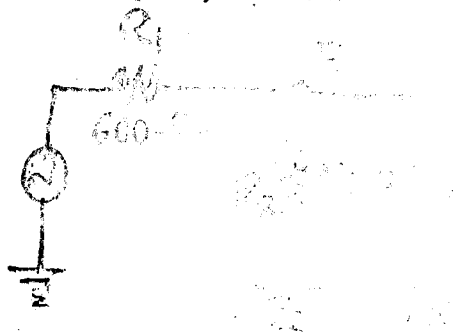


Fig. Q 3(b)

c. Write down the circuit diagram of a base – biased amplifier and its ac equivalent circuit replacing the transistor by its π model. (06 Marks)

4 a. Explain the working of an emitter follower circuit with its circuit diagram and its ac equivalent circuit. (06 Marks)

b. Distinguish between class A, class B, class AB and class C amplifier. (04 Marks)

c. Calculate the voltage gain and the ac voltage of the following emitter follower if $\beta = 150$.

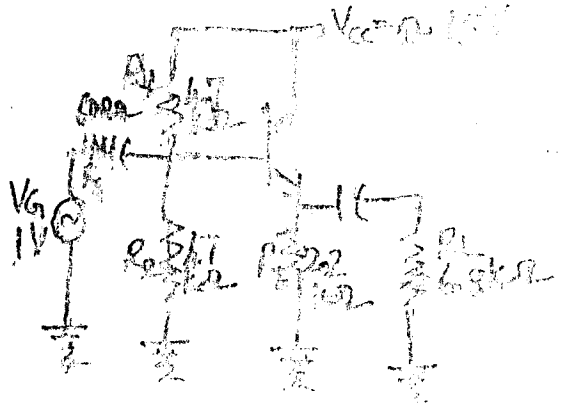


Fig. Q 4(c)

(10 Marks)

PART - B

5 a. Explain the structure of the depletion mode MOSFET. And the D – MOSFET curves. (10 Marks)

b. Explain the active load switching circuit using the MOSFET. Draw its equivalent circuit and its two terminal curves. (10 Marks)

6 a. Explain the frequency response of an amplifier. Describe the effect of the components that reduces the response of the amplifier below and above the midband. (08 Marks)

b. Explain the four types of negative feed back amplifiers. (12 Marks)

7 a. Draw the circuit diagram of an integrator and explain its operation with a typical input pulse. (10 Marks)

b. Draw and explain the circuit diagram of voltage controlled oscillator using the 555 timer. (10 Marks)

8 a. Define the terms 'Load Regulation' and 'Line Regulation' with respect to a power supply. (06 Marks)

b. Describe with circuit diagram, the operation of a shunt regulation power supply.

c. What are the advantages and disadvantages of shunt regulator? What are the advantages of a series regulator? (10 Marks)

*****

USN | | | | | | | | | | |

06CS32

Third Semester B.E. Degree Examination, Dec 08 / Jan 09
Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions selecting at least TWO from each part.***

PART – A

1 a. Define the condition for a stiff clipper and a stiff clamper. (02 Marks)

b. The circuit in fig.Q1.(b) a silicon diode IN314. From its data sheet the forward current is 10mA at 1V. Input signal is a sinusoidal wave of 10V peak to peak. What is the circuit? Find $R_{S(minimum)}$ and $R_{L(minimum)}$. What is $V_{out(max)}$ and $V_{out(min)}$. Sketch the output waveform. If the diode is reversed, what is $V_{out(max)}$ and $V_{out(min)}$. (08 Marks)

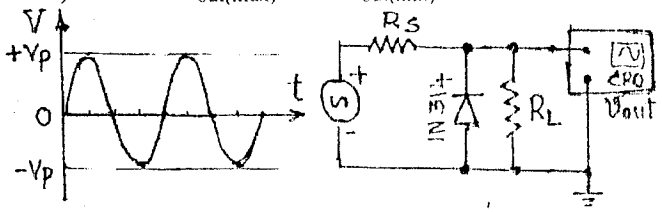


Fig.Q1(b)

c. What is an opto – electronic device? With the help of a simple circuit, explain the relationship between LED voltage, current and brightness. What is the condition for constant brightness of LED? What is the typical voltage drop across a LED? (06 Marks)

d. Describe how an LED is used as a Polarity Tester. (04 Marks)

2 a. Describe ac – short and ac – ground. (04 Marks)

b. What is the lowest frequency at which a good by passing exists in the circuit in fig.Q2(b)? (Hint Thevenin's Resistance). Given $R_1 = 2k\Omega$, $R_2 = 8\ k\Omega$ and $C = 100\mu F$. (04 Marks)

c. Fig. Q2(c) is a CE amplifier. Draw dc and π - model ac equivalent circuits. Calculate quiescent voltages and currents required, impedances of the input base and stage, voltage gain and output voltage. (12 Marks)

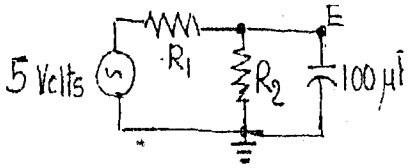


Fig.Q2(b)

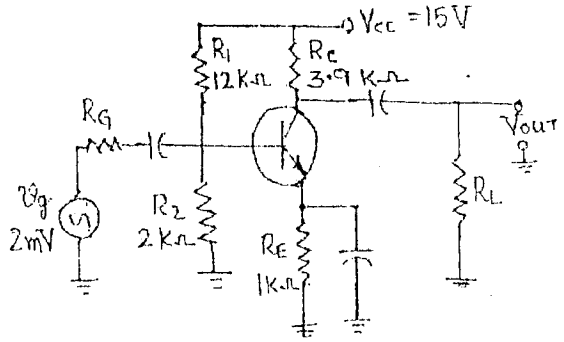


Fig.Q2(c)

3 a. With the help of a neat circuit diagram, explain two stage feed back and derive equation for voltage gain. (09 Marks)

b. Compare the characteristics of CE and CC amplifiers. (05 Marks)

c. In fig.Q3(c), find overall gain, base – current of Q1 and input impedance of base Q1, given $\beta 1 = \beta = 100$ as gain. (06 Marks)

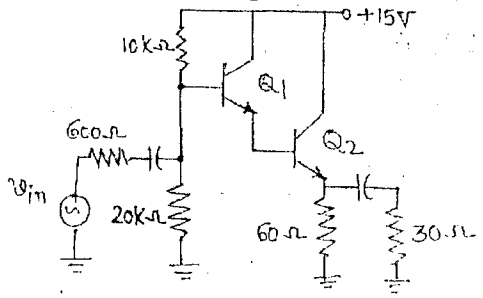


Fig.Q3(c)

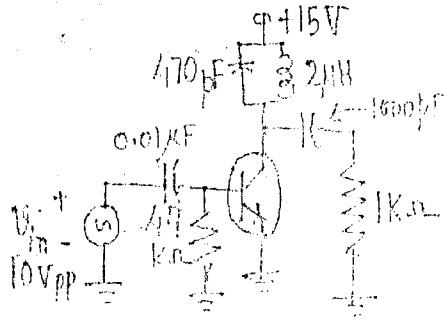


Fig.Q4(c)

4 a. Draw 'dc' Load Line and 'ac' Load Line for a VDB amplifier and derive equations for load lines. (08 Marks)

b. In a class 'C' amplifier define duty cycle, conduction angle and derive equation for 'ac' collector resistance. (06 Marks)

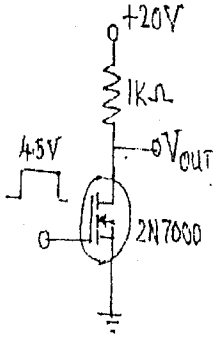
c. Fig.Q4(c) shows class C amplifier. Quality factor of coil $Q_L = 100$. What is the bandwidth of the amplifier? (06 Marks)

PART - B

5 a. With a neat sketch, explain the formation of an 'inversion layer' in a E - MOSFET. Draw and explain Drain and Transconductance curve of E – MOSFET. (10 Marks)

b. Explain biasing in ohmic range. (05 Marks)

c. In the circuit fig.Q5(c), what is the output voltage. (05 Marks)



From data sheet,
$V_{GS(ON)} = 4.5$ V
$I_D(ON) = 75$mA
$R_D(ON) = 6\Omega$

Fig. Q5(c)

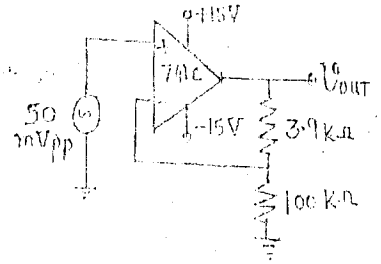


Fig.Q6(c)

6 a. Define Decibel voltage gain, Decade, Octave and PdBM. (04 Marks)

b. From data sheet, an op amp gives a mid – band voltage gain of 200,000, a cut – off frequency of 10 Hz and a roll off rate of 20 dB per decade. Draw the ideal Bode Plot. What is the Ordinary Voltage Gain? (08 Marks)

c. Calculate the feed back fraction, ideal closed loop voltage gain, the percent error and closed loop voltage gain, for the VCVS circuit in fig.Q6(c). Given typical A_{VOL} of 100,000 for the 741 C. (08 Marks)

7 a. Construct an Op-amp circuit to convert a sinusoidal wave to a rectangular wave form. Explain with relevant formulas, neat diagrams and waveforms. (10 Marks)

b. Using a 555 functional block, construct a monostable multi vibrator and explain its function. (10 Marks)

8 a. Draw simple sketches of IC Linear Regulators and IC switching regulators and compare their characteristics. (10 Marks)

b. Draw the circuit diagram of Zener and two transistor discrete series regulator and derive equation for the output voltage. (06 Marks)

c. Define Headroom and Power dissipation. (04 Marks)

*****

USN | | | | | | | | | | |

06CS32

Third Semester B.E. Degree Examination, June-July 2009
Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: *Answer FIVE full questions choosing at least two full questions from each part.*

Part A

1 a. Explain the working of positive clipper and negative clipper with circuit diagram. (06 Marks)

b. For the clipping circuit shown in figure, obtain the output voltage waveform assuming ideal diodes. Take $V_s = 40\sin\omega t$ (06 Marks)

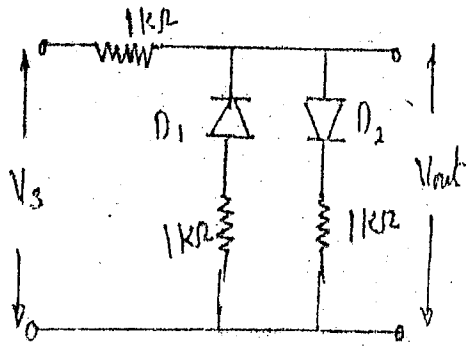


Fig. Q1 (b)

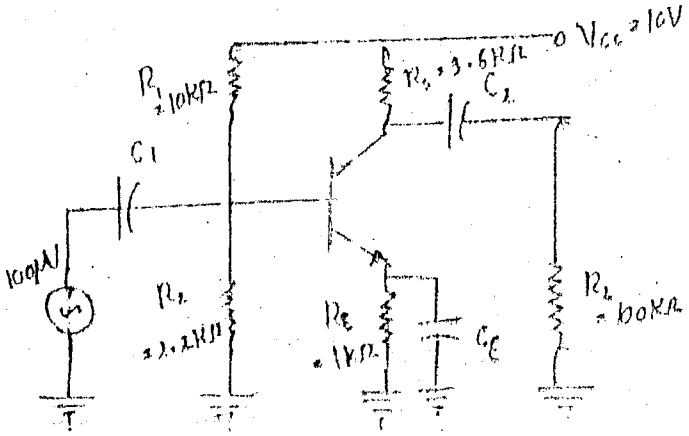


Fig. Q2 (a)

c. Explain the construction of SCHOTTKY diode along with its applications. (08 Marks)

2 a. Find the value of R_e' for the voltage divider bias amplifier shown in fig Q2 (a). If the emitter resistance is doubled, what is the OC resistance of emitter diode? $V_{BE} = 0.7$ V (10 Marks)

b. For the VDB amplifier shown below, draw the DC equivalent circuit and find the DC quantities I_E, V_E, V_{CE} and V_C. (10 Marks)

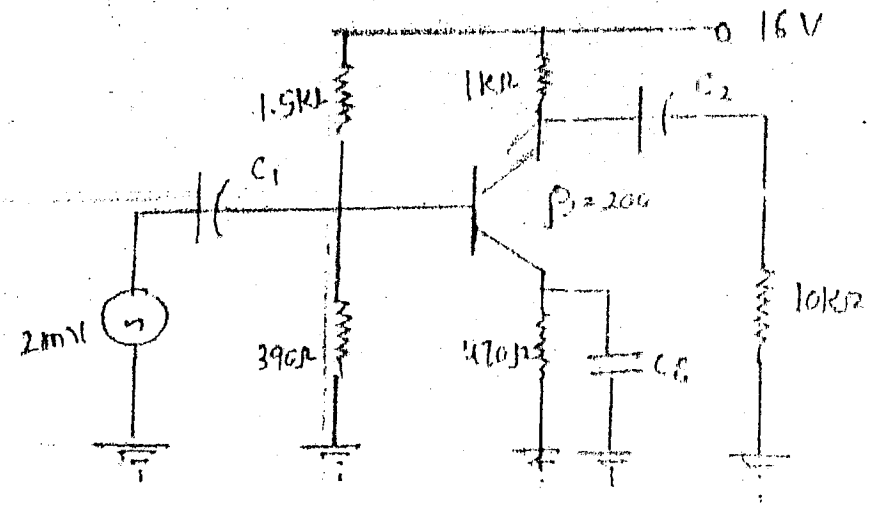


Fig. Q2 (b)

3 a. Explain, with the help of a circuit diagram, a two stage feedback amplifier. (10 Marks)

b. For the circuit shown below, calculate the value of output impedance. (10 Marks)

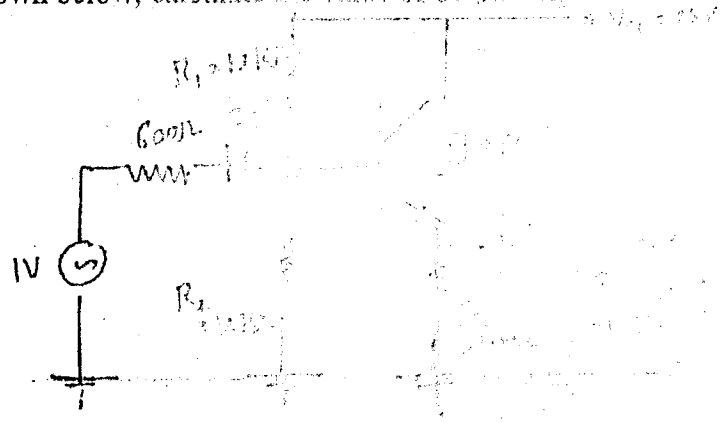


Fig. Q3 (b)

4 a. Explain the classification of amplifiers based on their operation. (08 Marks)

b. Show that the maximum efficiency of transformer coupled class A power amplifier is 50%. (12 Marks)

Part B

5 a. Explain the construction and principle of operation of enhancement mode MOSFET along with its drain and transconductance characteristics. (10 Marks)

b. Discuss in detail CMOS combiner n-channel and p-channel MOSFETs and hence explain CMOS power consumption. (10 Marks)

6 a. Discuss in detail the frequency response of RC and DC coupled amplifier. (10 Marks)

b. Explain the various types of negative feedback amplifier. (10 Marks)

7 a. Explain with a neat diagram comparator with non-zero reference voltage for positive and negative references. (10 Marks)

b. Explain with a neat circuit diagram the operation of a monostable multivibrator. (10 Marks)

8 a. Explain the various characteristics for the quality and suitability of power supply depends. (10 Marks)

b. For the shunt regulator shown in figure, V_{in} = 12 V, R_s = 20 Ω, V_Z = 5.6 V, V_{BE} = 0.8 V, R_2 = 50 Ω, R_1 = 1 kΩ, R_3 = 330 Ω, calculate

i) the output voltage ii) the input current

iii) the load current iv) the collector current

v) the approximate efficiency. (10 Marks)

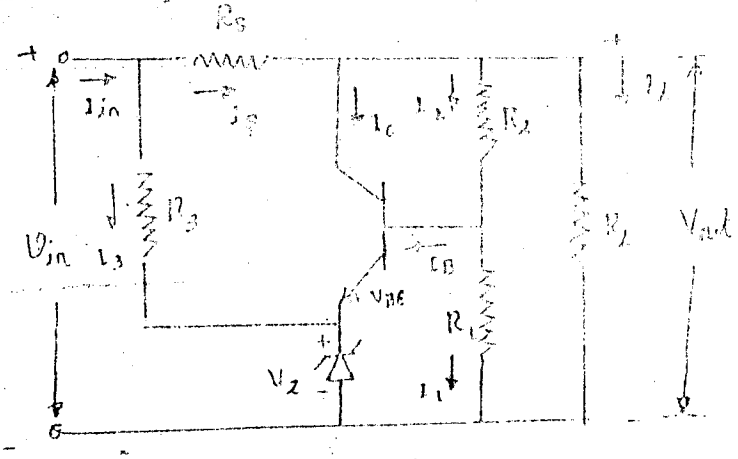


Fig. Q8 (b)

* * * * *

USN | | | | | | | | | | |

06CS32

Third Semester B.E. Degree Examination, Dec.09/Jan.10

Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With a neat diagram and waveforms, explain the working of a positive camper with respect to the stiff clamper condition. (08 Marks)

b. An LED is used in the indicator circuit for the a.c. power line of 230V AC with 50Hz frequency. The circuit consists of a capacitor of 0.68μf. Calculate the capacitive reactance and average LED current. (04 Marks)

c. Explain with relevant diagrams, the principle of operation of a varactor diode. (08 Marks)

2 a. Explain with a neat circuit diagram and a.c. equivalent circuit, the working of base biased amplifier. (08 Marks)

b. Sketch the output waveform for the clipper circuit of FigQ2(b) shown below. Assume silicon diode and obtain the peak magnitude of the output waveform.

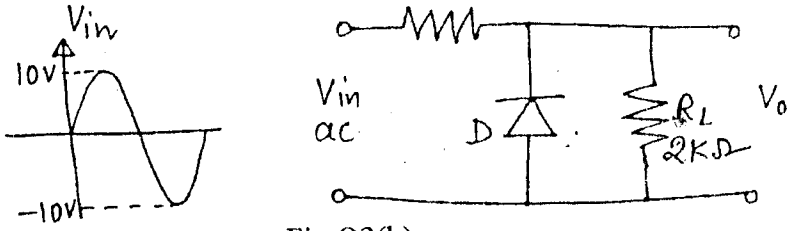


Fig.Q2(b) (06 Marks)

c. Find the voltage gain and output voltage across the load resistor for the given circuit of FigQ2(c).

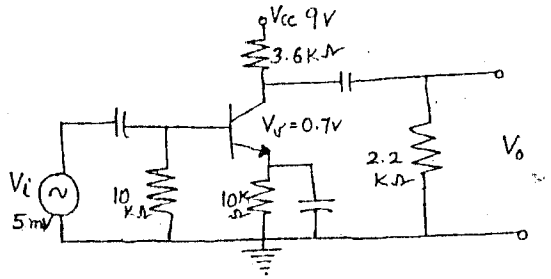


Fig.Q2(c) (06 Marks)

3 a. Explain the working of a swamped amplifier with a neat circuit diagram. Derive the expression for voltage gain. (08 Marks)

b. Draw the cascaded CE and CC stages of amplifier. Explain. (06 Marks)

c. Derive an expression for an output voltage for a series feedback type regulator. (06 Marks)

4 a. Explain the principal of operation of class B push-pull amplifier with a neat circuit diagram and relevant waveforms. (08 Marks)

b. In a class B amplifier, $V_{CE(min)}$ = 1 volt, supply voltage V_{CC} = 18 volts. Calculate the collector circuit efficiency. (04 Marks)

c. What is digital switching? Explain in detail passive load switching and active load switching. (08 Marks)

PART – B

5 a. What is impedance matching? Explain. (04 Marks)
b. Explain briefly decibel power gain and decibel voltage gain. (06 Marks)
c. Explain ideal closed loop voltage gain, gain stability, closed loop input impedance, closed loop output impedence and non linear distortion, with respect to VCVS amplifier. (10 Marks)

6 a. With relevant details, explain VCIS amplifier. (06 Marks)
b. Write a note on comparators with nonzero references. (06 Marks)
c. With a neat circuit diagram and waveforms, explain the sine wave to rectangular converter, using OP-AMP. (08 Marks)

7 a. Explain the principle of relaxation oscillator to generate rectangular output. Draw a neat circuit diagram and waveform. (08 Marks)
b. Explain with a neat connection diagram and waveforms, how IC555 timer is used as a stable multivibrator. (06 Marks)
c. What do you know about phase locked loops? Explain. (06 Marks)

8 Write an explanatory note on :
a. Opto electronic devices
b. Load lines in power amplifiers
c. Voltage controlled oscillator
d. Switching regulators. (20 Marks)

* * * * *

USN | | | | | | | | | | |

06CS32

Third Semester B.E. Degree Examination, May/June 2010
Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain positive clipper and negative clipper, with necessary diagrams. **(08 Marks)**

b. For the circuit shown in, Fig. Q1(b) :
i) Sketch the output voltage waveform ii) What is the maximum positive output voltage?
iii) What is the maximum negative output voltage? **(06 Marks)**

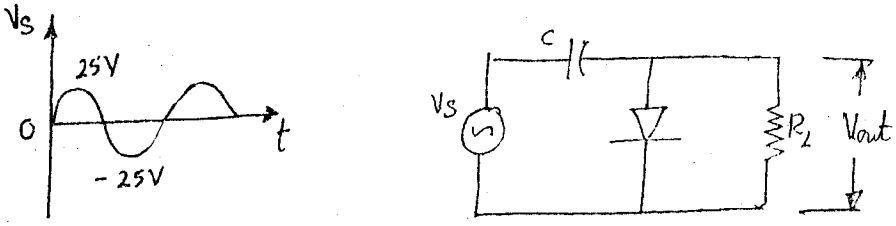


Fig. Q1(b)

c. Explain SCHOTTKY DIODE construction and its application. **(06 Marks)**

2 a. Explain with a neat circuit diagram, voltage divider bias amplifier by mentioning the importance of bypass capacitor. **(06 Marks)**

b. Obtain the graphical determination of AC emitter resistance of diode. **(06 Marks)**

c. Draw the DC and AC equivalent circuits of voltage divider bias amplifier shown in Fig. Q2(c). **(08 Marks)**

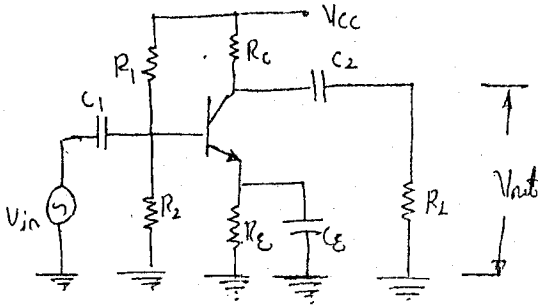


Fig. Q2(c)

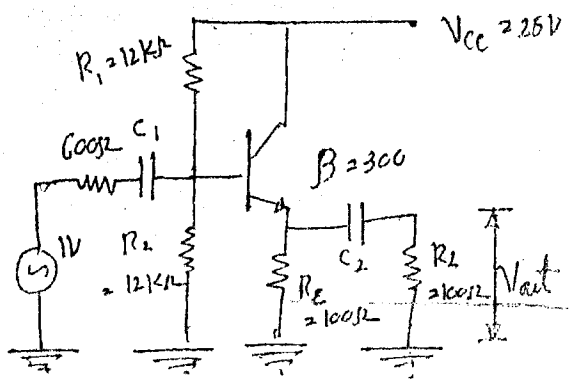


Fig. Q3(c)

3 a. Obtain the expression for voltage gain of single stage CE voltage-divider bias amplifier using π-model. **(08 Marks)**

b. Discuss trouble shooting of DC and AC circuits in voltage amplifier. **(06 Marks)**

c. For the circuit shown in, Fig. Q3(c), calculate the voltage of output impedance. **(06 Marks)**

4 a. Explain power gain interms of voltage and current gain in power amplifier. **(06 Marks)**

b. Show that the maximum efficiency of transformer coupled class A power amplifier is 50%. **(08 Marks)**

c. In a class C power amplifier V_{CC} = 30 V; R_L = 10 k Ω current drain I_{dc} = 0.4 mA peak–to–peak output voltage $V_{out(p-p)}$ = 30 V. Calculate i) DC input power ii) AC input power iii) Efficiency. **(06 Marks)**

PART – B

5 a. Explain the principle of operation and structure of n-channel depletion mode MOSFET, with a neat sketch. (06 Marks)

b. Discuss CMOS inverter with a neat circuit diagram, along with the transfer characteristics. (06 Marks)

c. Obtain the equation for voltage gain of common-source D-MOSFET amplifier. (08 Marks)

6 a. Explain the frequency response of a typical AC amplifier, mentioning the importance of cut-off frequency. (08 Marks)

b. Obtain the formula for decibel power gain and decibel voltage gain. (04 Marks)

c. For the circuit shown in Fig. Q6(c). Calculate :
i) The feedback fraction ii) The ideal cloud leep voltage gain iii) The exact-cloud leep voltage gain iv) The percentage error between ideal and exact valves of the closed leep voltage gain. Assume the open leep voltage gain of op. amp as 10^5. (08 Marks)

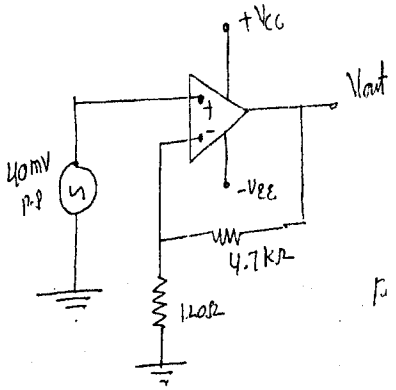


Fig. Q6(c)

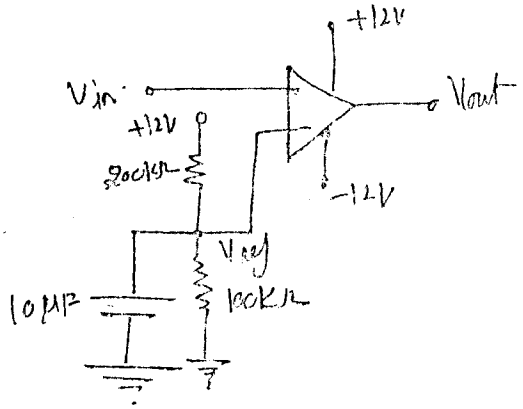


Fig. Q7(b)

7 a. Explain the functional block diagram, of 555 timers. (08 Marks)

b. The input voltage to the circuit shown in, Fig. Q7(b) is a sine wave of peak value 8V.
i) Calculate the trip point or threshold ii) Calculate the cut-off frequency of the bypass circuit iii) Sketch the output waveform and determine its duty circle. (08 Marks)

c. Explain how Schmitt trigger can be used to convert a periodic sine wave to a rectangular wave. (04 Marks)

8 a. Explain the various characteristics on which a power supply depends, with respect to quality and suitability : (04 Marks)

b. Calculate the output voltage for the circuit shown below in the Fig Q8(b) : (08 Marks)

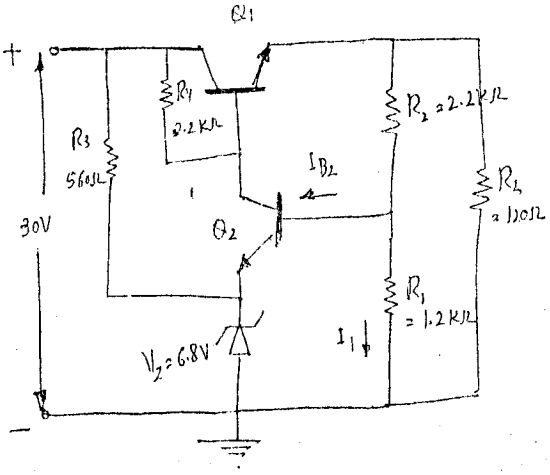


Fig. Q8(b)

c. Explain with a circuit diagram, unregulated DC to DC converter using power BJTs. (08 Marks)

* * * * *